Self-Assembled Incorporation of Modulated Block Copolymer Nanostructures in Phase-Change Memory for Switching Power Reduction

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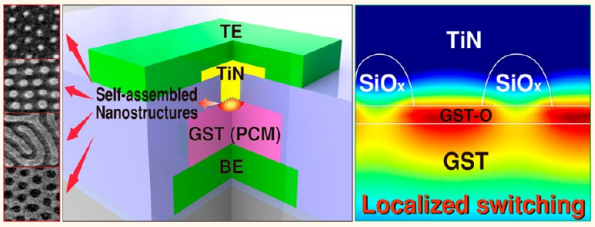
ABSTRACT Phase change memory (PCM), which exploits the phase change behavior of chalcogenide materials, affords tremendous advantages over conventional solid-state memory due to its nonvolatility, high speed, and scalability. However, high power consumption of PCM poses a critical challenge and has been the most significant obstacle to its widespread commercialization. Here, we present a novel approach based on the self-assembly of a block copolymer (BCP) to form a thin nanostructured SiO_x layer that locally blocks the contact between a heater electrode and a phase change material. The writing current is decreased 5-fold (corresponding to a power reduction by 1/20) as the occupying area fraction of SiO_x nanostructures is increased from a fill factor of 9.1% to 63.6%. Simulation results theoretically explain the current reduction mechanism by localized switching of BCP-blocked phase change materials.



KEYWORDS: block copolymers · self-assembly · phase change memory

Phase change memory (PCM) is one of the most promising candidates for universal nonvolatile memory and a key component of portable electronic devices.[1−3] In order to be used as a core memory for mobile devices, its writing current should be minimized below at least one-third of its present level.[1,4,5] The writing current of PCM scales with the switching volume of the phase change material, and thus the power consumption per cell diminishes with a decrease of cell size.[6−8] However, the scaling-down of memory devices is becoming more challenging due to the diffraction limitation of optical lithography.[1] Novel and useful approaches that are applicable independently of a given technology node should thus be sought. Although there have been many attempts to reduce the writing current, including the engineering of materials, structures (U-cup, edge contact, ring-type, *etc.*), and interfaces,[6,9−14] sufficient power reduction has not been achieved.

Block copolymer (BCP) self-assembly, which is driven by the microphase separation of two mutually incompatible blocks, can create ordered arrays of sub-20 nm features.[15−24] BCP self-assembly is now considered to be a viable route to sub-16 nm lithography nodes due to its excellent resolution, scalability, and compatibility with the conventional CMOS process.[1,20,21,23−29] We have previously reported the large-area fabrication of oxide and metallic nanostructures such as wires, dots, and rings with an exceptional degree of long-range ordering and tunability using Si-containing BCPs.[18−20,32,33] Although previous studies demonstrated the memory characteristics of various nanostructures prepared from BCP nanotemplates without using high-cost nanolithography,[34−38] the key distinction of this study is that the dramatic performance enhancement of near-commercialized nonvolatile memory devices is achieved using the self-assembly technology. We show how a bottom-up

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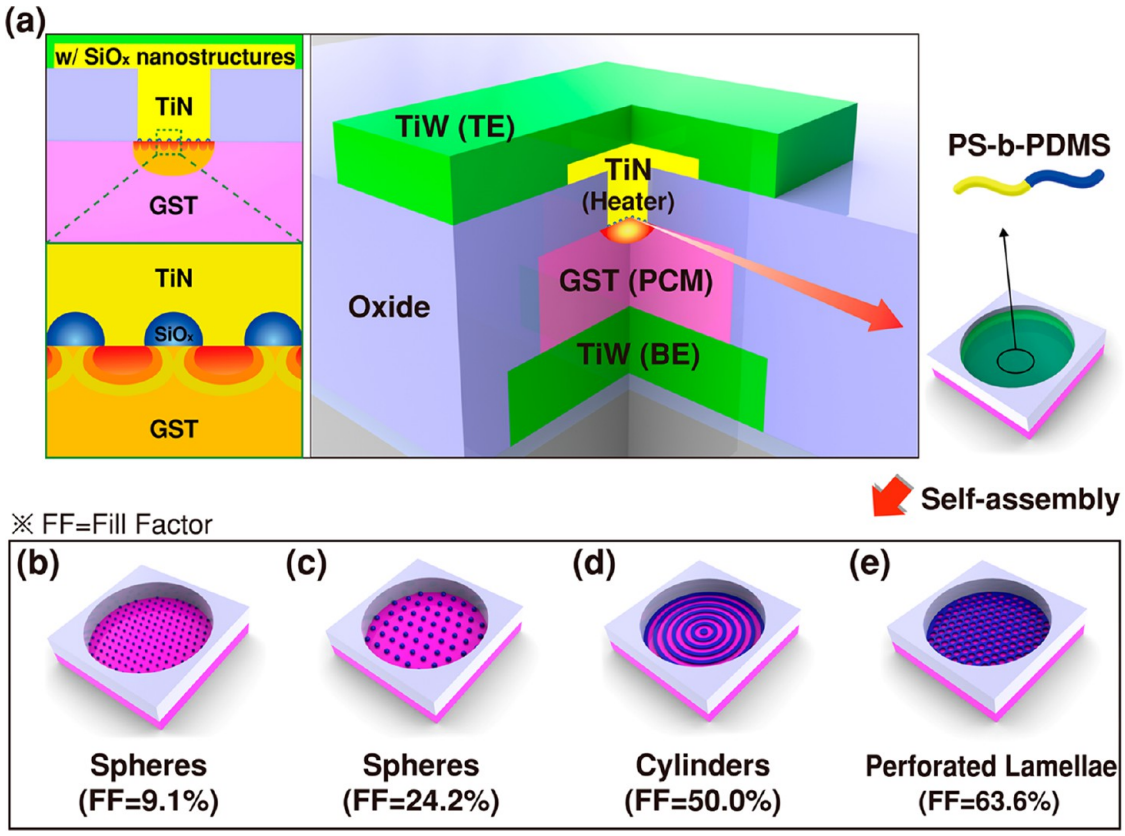

Figure 1. PCM devices and current-blocking SiO_x nanostructures. The morphologies and fill factors (FF) of the nanostructures were controlled using the self-assembly of Si-containing PS-*b*-PDMS block copolymers. (a) Schematic of the PCM device structure. (b–e) Different morphologies of the self-assembled nanostructures between GST and TiN. (b) Small spheres (FF = 9.1%), (c) large spheres (24.2%), (d) cylinders (50.0%), and (e) hexagonally perforated lamellae (HPL) (63.6%).

approach can resolve the chronic issue of power consumption in phase change memory independently of shrinking the memory cell size.

In this study, the interface between the phase change material and the heater electrode is engineered by incorporating insulating silica nanostructures. Our simulation results suggest that the switching volume of the phase change material can be reduced without requiring expensive advanced nanolithography. The reset current of PCM devices decreases in proportion to the reduction of the contact area between a phase change $Ge_2Sb_2Te_5$ (GST) thin film and a TiN resistive heater.[39] Contact between GST and TiN is made only in the open region (*e.g.*, hole) without the SiO_x nanostructures. In order to control the contact area effectively, we employed the self-assembly of Si-containing poly(styrene-*b*-dimethylsiloxane) (PS-*b*-PDMS) BCPs, whose fill factor and pattern geometry could be tailored over a wide range at the interface between a GST and a TiN (Figure 1a). The self-assembled PDMS microdomains can easily be converted into thermally stable and insulating SiO_x nanostructures after a short reactive ion etch (RIE) with an O_2 plasma.[15,17,18,40] Alternatively, various additional insulating oxide nanostructures can be formed by other pattern transfer techniques such as sequential infiltration synthesis (SIS).[41] Furthermore, the geometries and area fill factors of the SiO_x nanostructures can be easily controlled by changing the molecular weight (MW) of BCPs and the parameters of solvent vapor annealing.[18,22] Thus, as schematically shown in Figure 1b–e, various SiO_x nanostructures with tailored geometries and area filling factors were generated on GST thin films, enabling the effective control of temperature distributions in a PCM device.

RESULTS AND DISCUSSION

First, we demonstrate how the geometries and fill factors of blocking oxide nanostructures on GST thin films can be controlled. Fill factor is defined as the occupying area fraction of SiO_x nanostructures on GST film, and the contact area between GST and TiN is decreased by increasing the fill factor. Scanning electron microscopy (SEM) images of self-assembled SiO_x nanostructures formed within the circular hole of a PCM device are shown in Figure 2. The long-range uniformity of the SiO_x nanostructures was previously confirmed by grazing-incidence small-angle X-ray scattering (GISAXS).[17] The SiO_x nanostructures were obtained from BCPs forming spherical (Figure 2b and c), cylindrical (Figure 2d), and hexagonally perforated lamellar (HPL) (Figure 2e) morphologies, and their fill

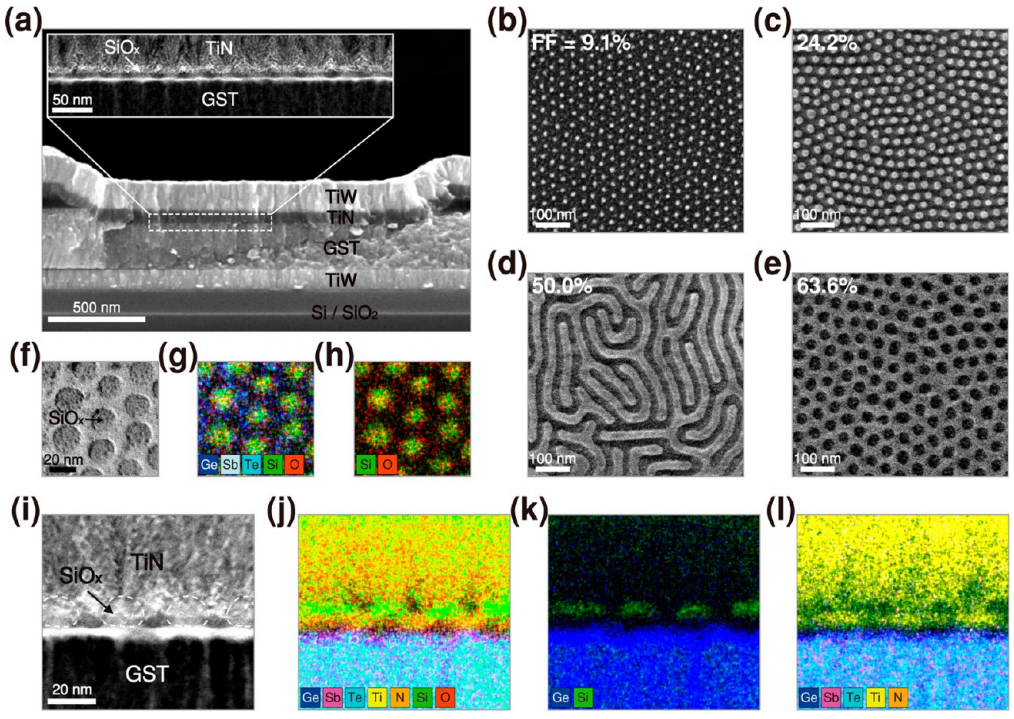

Figure 2. SEM and TEM analyses. (a) Cross-sectional SEM images of the PCM device. The inset shows a TEM image of the interface between TiN and GST, where the self-assembled nanostructures are incorporated. (b–e) SEM images of the self-assembled nanostructures on GST thin films. (b) Small spheres (FF = 9.1%), (c) large spheres (24.2%), (d) cylinders (50.0%), and (e) hexagonally perforated lamellae (HPL) (63.6%). (f) Top-down bright-field TEM image of the SiO_x nanodots on GST. (g and h) EDS elemental mapping results of (g) Ge, Sb, Te, Si, and O and (h) Si and O. (i) Cross-sectional TEM image at the interface. (j–l) EDS elemental mapping results of (j) Ge, Sb, Te, Ti, N, Si, and O, (k) Ge and Si, and (l) Ge, Sb, Te, Ti, and N.

factors were 9.1%, 24.2%, 50.0%, and 63.6%, respectively. These four morphologies were made from three kinds of PS-*b*-PDMS BCPs with different MWs of 50–5, 43–8.5, and 31–14.5 kg/mol, which have PDMS volume fractions (f_{PDMS}) of 9.8%, 17.7%, and 33.7%, respectively. Among the various morphologies, the cylindrical and HPL nanostructures were obtained from one BCP (31–14.5 kg/mol) by changing the solvent vapor annealing conditions using mixed solvents (Figure S2). The morphology and fill factor of the self-assembled nanostructures are governed primarily by the volume fraction of the component blocks and by the MW. However, the additional control of feature size and fill factor can be obtained using a solvent-annealing method in which the film is exposed to mixtures of vapors of two preferentially segregating solvents and in which the preferential swelling of one block is achieved.[18] After spin-coating BCP solutions dissolved in toluene, the samples were solvent-annealed in a chamber at 25 °C for two hours. However, the self-assembly kinetics can be significantly accelerated by increasing the solvent-annealing temperature, and well-defined BCP nanostructures can be obtained even in one minute of self-assembly time, as we recently reported.[42] The self-assembled polymer nanostructures were then converted into SiO_x nanostructures by plasma oxidation. These processes produced a wide range of geometries, as shown in Table 1, by affording control over the MW and solvent-annealing parameters of the BCPs.

TABLE 1. MW of the BCPs, Annealing Conditions, and Fill Factors for Various Self-Assembled Morphologies

MW [kg/mol]	f_{PDMS} [%]	annealing vapor	morphology	fill factor [%]
55	9.8	toluene	spheres	9.1
51.5	17.7	toluene	spheres	24.2
45.5	33.7	toluene	cylinders	50.0
45.5	33.7	toluene + heptane	HPL	63.6

The uniform incorporation of the self-assembled oxide nanostructures between the GST and TiN layers without significant variation of the geometry and size was confirmed through transmission electron microscopy (TEM) analyses. Top-view TEM (Figure 2f) and energy dispersive spectroscopy (EDS) elemental mapping images (Figure 2g and h) present well-defined SiO_x nanodots on a GST thin film. A cross-sectional bright-field TEM image shows SiO_x nanodots between GST and TiN (Figure 2i), and EDS elemental mapping analysis results in Figure 2j, k, and l show the successful formation of silica nanostructures between the phase-changing active material and the heater electrode. The self-assembled current-blocking nanostructures locally reduce the contact area and lead to significant power reduction by decreasing the area over which current flows.

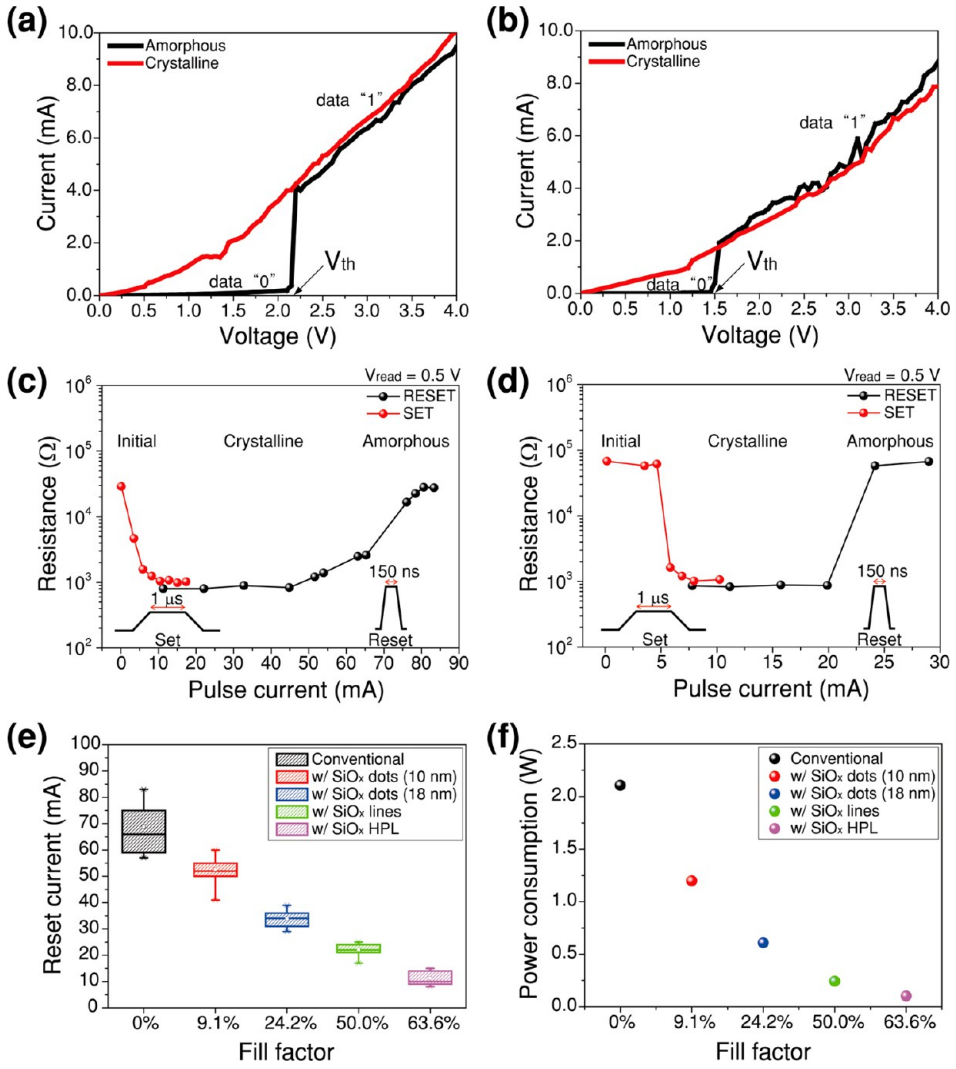

Figure 3. Electrical measurement results of the PCM devices with/without self-assembled SiO_x nanostructures. (a) *I*−*V* and (c) *R*−*I* curves of the PCM device without nanostructures (conventional cell). (b) *I*−*V* and (d) *R*−*I* curves of a cell with SiO_x nanostructures (FF = 50%). (e) Reset current *versus* fill factor, showing a proportional decrease of switching current with an increase of fill factor. (f) Switching power *versus* fill factor. The pulse widths for SET and RESET operations were set to be 1 μs and 150 ns, respectively.

To investigate the performance improvement of a phase-change memory by incorporation of self-assembled SiO_x nanostructures, electrical tests were performed using a semiconductor parameter analyzer and a pulse generator. The procedure for fabricating PCM devices is schematically illustrated in Figure S1 in the Supporting Information. Voltage pulses were applied to the bottom electrode (TiW), while the top electrode (TiW) was grounded. For the conventional device without any self-assembled nanostructures, current−voltage (*I*−*V*) and resistance−current (*R*−*I*) curves indicate that the threshold switching, RESET, and SET voltages were 2.2, 27, and 5 V, respectively, and its reset current was estimated to be 75 mA (Figure 3a and c). On the other hand, for the device with silica nanostructures with an area fill factor of 50.0%, the threshold switching, RESET, and SET voltages were decreased to 1.5, 10, and 3 V, respectively, and the reset current was reduced to 24 mA (Figure 3b and d). By locating SiO_x nanostructures at the interface, the direct contact area between GST and TiN decreased significantly, resulting in a reduction of the threshold switching voltage and reset current (less than one-third of the reset current for the conventional cell). In addition, further work was conducted to confirm the effectiveness of this technology for a submicrometer PCM device with a contact area of 500 × 500 nm^2. The reset current was reduced 4-fold for the device with a fill factor of 63.6%. These results indicate that our approach of power reduction based on BCP self-assembly is applicable independently of device feature size and technology node. As we previously reported, the self-assembled SiO_x nanostructures can be formed in circular trenches with a sub-50 nm diameter,[19] and it is therefore expected that the power-reduction mechanism can be implemented for the current state-of-the-art PCM technology.

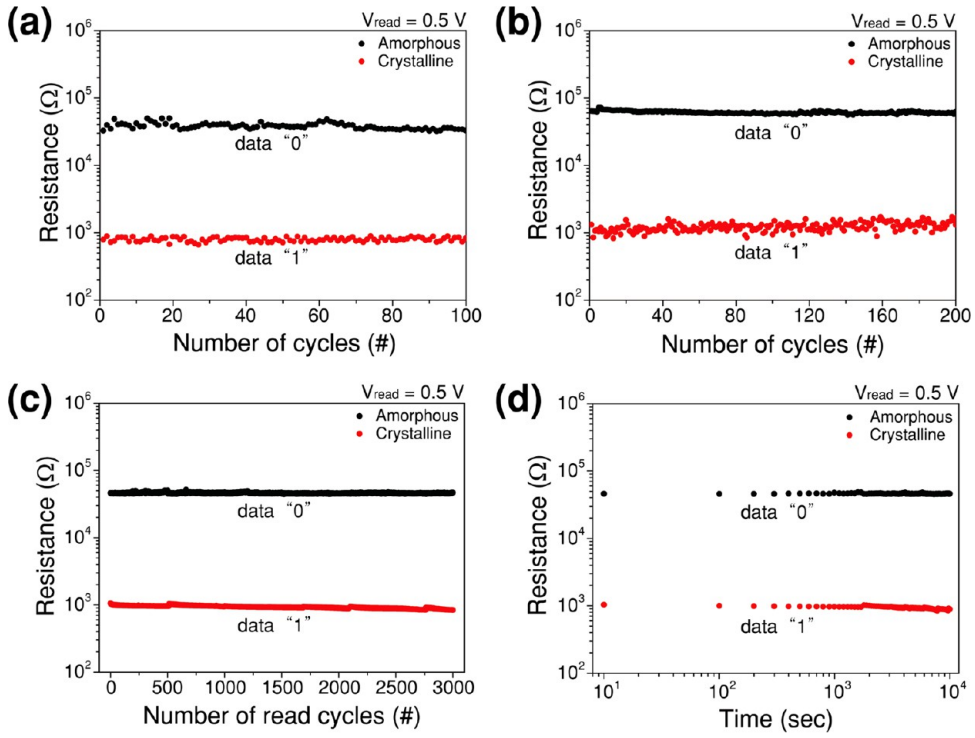

Figure 4. Device reliability evaluations. Write endurance of the PCM device (a) without and (b) with SiO_x nanostructures (FF = 50%). (c) Read endurance and (d) retention time results of the PCM cells with SiO_x nanostructures (FF = 50%).

The resistance ratios between the amorphous (RESET) and crystalline (SET) states remained constant regardless of fill factors. In order to observe the dependence of the reset current and the performance distribution on the contact area, PCM devices with different fill factors were measured. Figure 3e presents the cell-to-cell variations of PCM devices and the trends of the reset current with different fill factors. The small device-to-device variation in the reset current for the BCP-modified PCM devices can be attributed to the good and reproducible uniformity of the self-assembled nanostructures. The switching power per cell required for reset operation is proportional to the reset current (I_r) and cell resistance (R_c): $P \propto I_r^2 R_c$.[12] Therefore, the power consumption required to amorphize the crystalline GST also decreases from 2.1 W to 0.10 W (approximately 20-fold power reduction) with an increasing fill factor (Figure 3f). As a result, the switching power shows an empirical dependence on the fill factor, delineated as $P \approx (1 - \mathrm{FF})^{2.84}$ (Figure S5).

The endurance and retention properties of PCM devices with self-assembled nanostructures were evaluated to identify whether this approach can maintain the reliability of PCM devices, showing an on/off resistance ratio of up to $\sim 10^2$, which is comparable to previous studies.[9,11,39] PCM cells containing self-assembled SiO_x nanowires with a fill factor of 50.0% exhibited good stability upon repeated switching, showing at least 200 write cycles by repetitive RESET/SET operations at a read voltage of 0.5 V (Figure 4b). During the 200 cycles, the two states maintained their resistance values without significant degradation, similarly to the device without the silica nanostructures (Figure 4a). Furthermore, the read endurance test results show excellent stability of around 3×10^3 read cycles at a read voltage of 0.5 V (Figure 4c). It also showed stable retention of up to 10^4 s at room temperature (Figure 4d).

In order to investigate the mechanism of the enhanced behavior, the PCM devices were simulated using the electrothermal method, in which two coupled equations were solved by finite element analysis to know the heat generated by Joule heating and the temperature distribution caused by heat transfer in the device.[43] The mathematical model for heat transfer by conduction is heat equation

$$\rho C \frac{\partial T}{\partial t} - \nabla(k\nabla T) = Q \qquad (1)$$

where ρ is the density, T is the temperature, C is the heat capacity, k is the thermal conductivity, t is the time, and Q is the heat flux.[44] The heat generated by Joule heating Q is given by

$$Q = \frac{1}{\sigma}|J|^2 = \sigma|\nabla V|^2 \qquad (2)$$

where σ is the electric conductivity, J is the electric current density, and V is the electric potential. For the simulations, we calculated the temperature profile in the GST from the switching current values obtained from measurements of the PCM devices. The existence of the self-assembled nanostructures resulted in

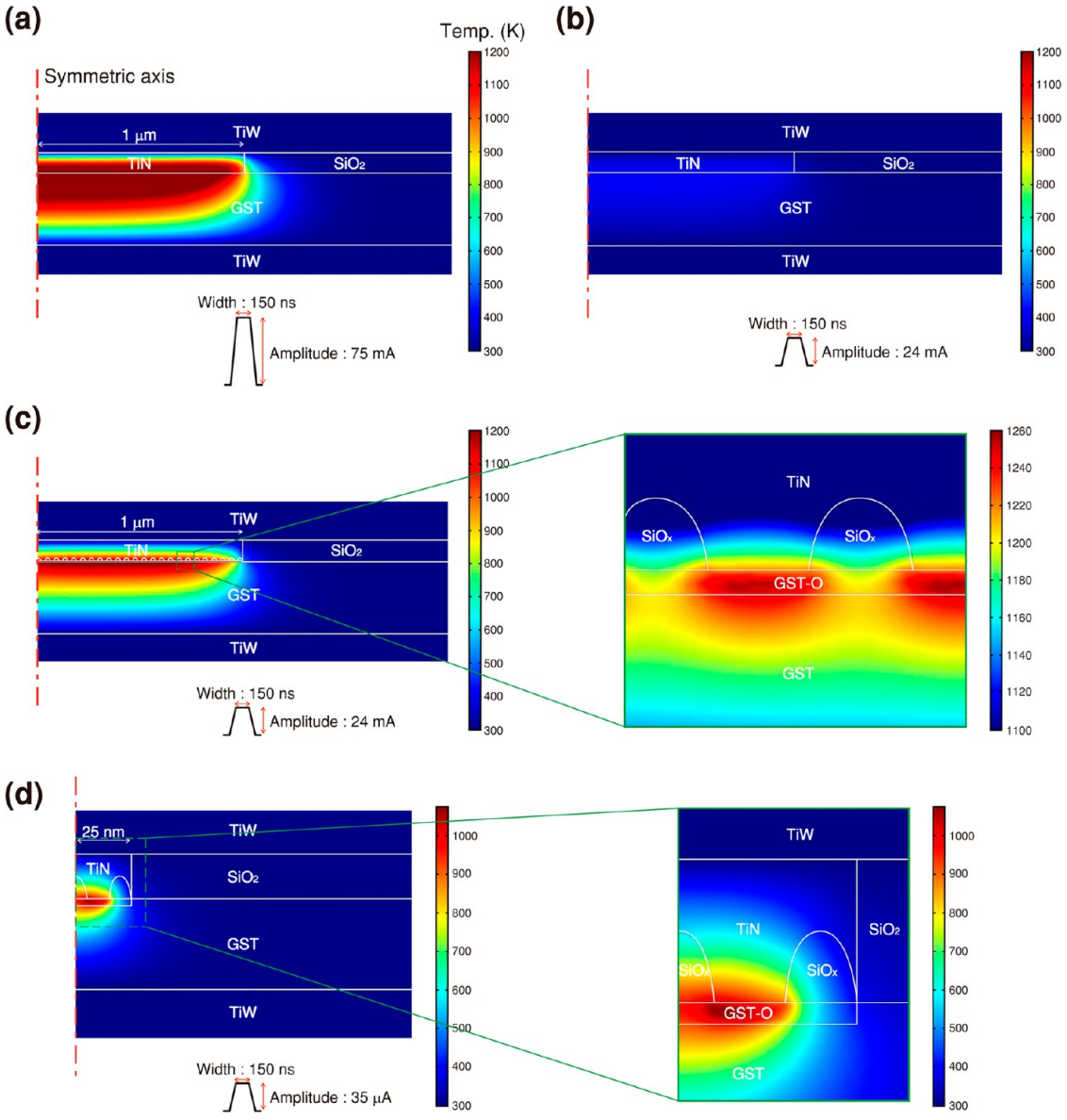

Figure 5. Temperature distributions in PCM cells calculated by electrothermal simulations. The contact hole sizes were fixed at 2 μm except in the case of (d). (a and b) Without SiO_x nanostructures. Current pulses of (a) 75 mA and (b) 24 mA. (c) With the SiO_x nanostructures (FF = 50%) and an applied current pulse of 24 mA. (d) For the device with SiO_x nanostructures with a much smaller cell size (contact hole diameter = 50 nm).

significantly modified temperature distributions in the GST film. For the cell without the silica nanostructures, when a reset current pulse of 75 mA (the minimum switching current measured for the conventional cell) was applied with a duration of 150 ns, the maximum temperature of the GST film was calculated to be 1330 K (Figure 5a), which is above the melting point (T^{melt} = 888 K) of GST.[45] A lower reset current of 24 mA failed to increase the temperature over 404 K, as shown in Figure 5b, and thus reset switching was impossible at this lower current. In contrast, for the PCM structure containing the SiO_x nanostructures (FF = 50%), the low current (24 mA) resulted in a maximum temperature of 1261 K (Figure 5c), which is sufficiently higher than T^{melt} of GST for the cell to be reset. The magnified view shown in Figure 5c presents the effective role of the current-blocking SiO_x nanostructures for the modification of the temperature profiles and the reduction of switching volume in the GST film. The switching volume of the cell with the silica nanostructures calculated from the area fraction of the GST that reached $T > T^{melt}$ (888*K*) is estimated to be about 48% of the conventional device. This suggests that the reduction of switching power by the nanostructures is a result of the reduced switching volume. These simulation results support the experimental power reduction shown in Figure 3. Furthermore, the simulation indicates that this methodology would also work for devices fabricated with much smaller design rules. Similar localized heating effects and the reduction of switching current by the nanostructures

were reproduced well for a cell with a 50 nm wide contact hole, shown in Figure 5d and Figure S6.

CONCLUSIONS

We introduced a novel approach that shows how the switching power of PCM devices can be effectively reduced 20-fold by incorporating one simple step based on a BCP self-assembly process. The BCP-modified memory technology was successfully implemented in the PCM device, providing substantial power reduction, independently of cell size. These results are highly meaningful in that significant power reduction can be achieved without using high-cost lithographic tools to reduce memory cell size. The simulation results in this study and our previous report on successful BCP patterning[19] suggest that this approach can be applied to the state-of-the-art sub-50 nm PCM devices and may also be extendable to other nonvolatile memory devices such as resistive random access memory.[46]

METHODS

BCP Self-Assembly. To promote the self-assembly of BCPs, the surface of the $Ge_2Sb_2Te_5$ film was functionalized with a hydroxy-terminated homopolymer (PS-OH, MW = 22 kg/mol) at 150 °C for 2 h under vacuum and washed with toluene to remove unreacted polymers. Then, 1.2 wt % solutions of the BCPs dissolved in toluene were spin-cast on the brush-coated GST film. In order to form uniformly monolayered SiO_x nanostructures on the GST film, the thickness of the BCP film was optimized to be 25−35 nm depending on the MW of the BCPs. The BCPs were annealed at 85 °C under pure toluene or mixed vapors of heptane and toluene. The annealed samples were treated with CF_4 plasma (21 s at 50 W) followed by O_2 plasma (25 s at 60 W) using a reactive ion etching system, resulting in various self-assembled SiO_x nanostructures. During the plasma oxidation, the PS brush layer on the GST film was also completely removed.

PCM Device Fabrication. Si samples with 150 nm thick SiO_2 were used as substrates. The TiW bottom electrode (150 nm) and $Ge_2Sb_2Te_5$ active layer (350 nm) were formed by radio frequency (RF) sputter deposition. A SiO_2 insulator layer with a thickness of 100 nm was prepared by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C. A 2 μm diameter hole for the contact was lithographically patterned using a mask aligner (MDA-8000B) and RIE with C_4F_8 gas, and the BCP self-assembly process was performed. Then, a TiN heating layer (100 nm) was deposited on the $Ge_2Sb_2Te_5$ films with and without the SiO_x nanostructures, and a TiW top electrode (200 nm) was deposited and patterned.

Electrical Measurements. All the electrical measurements were performed in ambient conditions by using a Keithley 4200-SCS (dc voltage sweep), a Keithley 4225-PMU (pulse generator, waveform capture of current, voltage, and resistance), a 4225-RPM (remote amplifier/switches), and a probe station. The resistances of the devices were measured at a read voltage of 0.5 V.

TEM Measurements. Cross-sectional transmission electron microscopy samples were prepared by mechanical polishing, followed by ion milling with Ar ions. Bright-field TEM (BFTEM) and high-resolution TEM (HRTEM) studies were performed using a JEOL JEM-ARM200F microscope operated at 200 kV.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Supplementary figures. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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